CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

AMENDMENTS TO THE CLAIMS

1 - 18. (Cancelled)

19. (Previously Presented) A method of controlling a processor within a data processing system, comprising:

maintaining said processor in a halt condition in response to reset information from said data processing system;

stopping an execution cycle of said processor;

releasing said processor from said halt condition, said execution cycle remaining stopped;

configuring at least one memory resource in communication with said processor after the processor is released from the halt condition and while the execution cycle of the processor is stopped; and

starting said execution cycle of said processor.

20. (Original) The method of claim 19, wherein said configuring step comprises:

storing data in said at least one memory resource at a location associated with a reset vector of said processor.

21. (Original) The method of claim 20, wherein said data comprises code configured to be executed by said processor.

22. (Original) The method of claim 20, wherein said processor is started in response to storage of said data.

23. (Original) The method of claim 19, wherein said configuring step comprises:

storing data in said at least one memory resource at a location; and

setting a program counter of said processor to said location.

24. (Original) The method of claim 19, wherein said processor is embedded within an integrated circuit, and wherein said reset information is generated in response to initialization of said integrated circuit.